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CS 152 Computer Architecture and Engineering Final Exam SOLUTIONS May 12, 2020 Professor Krste Asanovi Name:_____ SID:_____ I am taking CS152 / CS252 (circle one) 180 Minutes, 27 pages. Notes: • Not all questions are of equal difficulty, so look over the entire exam!

CS 152 Computer Architecture and Engineering Final Exam ...

Computer Architecture Final Exam Solutions CSE 30321 – Computer Architecture I – Fall

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2010 Final Exam December 13, 2010 Test Guidelines: 1. Place your name on EACH page of the test in the space provided. 2. Answer every question in the space provided. If separate sheets are needed,

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Computer Architecture - Instructions 1. Write your name now. Name: Final Exam A simple (No wireless) calcu- 2. 3. 4. 5. 6. 8. Maximum score: 115. This exam is open book and open notes. lator is allowed. You should have 6 questions in 16 pages. Exam length: 2 hours. Read all the questions before you begin. Show all your work. Write clearly.

FINAL EXAM3 - Department of Electrical & Computer Engineering

EE321: Computer Architecture Final Exam Solution (1h30) 2017 – 2018 Notes : Answer briefly and clearly using the provided space. No extra sheet will be accepted. 1. Interrupts (5 pts) Consider a system with 3 I/O devices: D1, D2, and D3, with increasing priorities of 1 (low priority), 2 and 3 (high priority), respectively.

EE321: Computer Architecture Final Exam Solution (1h30 ...

CSE 30321 – Computer Architecture I – Fall 2010 Final Exam December 13, 2010 Test Guidelines: 1. Place your name on EACH page of the test in the space provided. 2. Answer every question in the space provided. If separate sheets are needed, make sure to include your name and clearly identify the problem being solved. 3. Read each question ...

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CSE 30321 – Computer Architecture I – Fall 2010 Final Exam ...

Computer Architecture 1 Fall 2011 Final Exam Solutions, Uppsala University Page 3 of 8
MIPS&Assembly&[12points]& 5a. Write MIPS assembly for the algorithm below. [4 points] $c = a + b + 4$; do { $c -= a$; $b++$; } while ($c > 3$) a is in $\$t0$, b is in $\$t1$, c is in $\$s0$. Clear comments are required for each line of code. Code Comments

Dark 1 HT2011 Exam Solutions - Uppsala University

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CSE 490/590 Computer Architecture Midterm Solution DIRECTIONS Time limit: 45 minutes (12pm - 12:45pm) There are 40 points plus 5 bonus points. This is a closed-book, no calculator, closed-notes exam. Each problem starts on a new page. Please use a pen, not a pencil. If you use a pencil, it won ' t be considered for regrading.

CSE 490/590 Computer Architecture Midterm Solution

EXAM 1 SOLUTIONS Assume we would like to use the exact same solution (history buffer) for executing a store instruction to memory. Why is this difficult to do? It is difficult to UNDO the effect of a store instruction. Another processor might read and use the value supplied by the store instruction before the store is undone.

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EXAM 1 SOLUTIONS - Electrical and Computer Engineering

This means that the computer (CPU) will seem faster to the user with more RAM to keep more data and instructions close at hand for the CPU. Hardware D 19 Yes. Thumb Drives (a.k.a. USB keys) offer more storage and quicker data access in a smaller, more convenient package. Most PC makers have stopped including diskette drives as standard PC ...

Answers to Chapters 1,2,3,4,5,6,7,8,9 - End of Chapter ...

Title: Dark 1 HT2011 Exam Solutions Author: David Black-Schaffer Created Date: 1/6/2012 12:07:31 PM

Dark 1 HT2011 Exam Solutions - Uppsala University

Reading: Essentials of Computer Architecture Chapter 18. Question and Answer session, catch-up, review, or topic of your choice. Please email suggestions. Course review, prepare for final exam (a draft solutions). Assignment 5 Solutions; Assignment and Lab schedule on WebCT. Final exam (draft solutions), Monday, April 30, 2007, 19:00-21:00, SC 239.

CS 250: Computer Architecture

18-447 Intro to Computer Architecture, Spring 2012 Final Exam Instructor: Onur Mutlu

Teaching Assistants: Chris Fallin, Lavanya Subramanian, Abeer Agrawal Date: May 10, 2012

Name: SOLUTIONS Problem I (190 Points) : Problem II (60 Points) : Problem III (60 Points) : Problem IV (30 Points) : Problem V (45 Points) : Problem VI (60 Points) :

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Name: SOLUTIONS - Electrical and Computer Engineering

CMSC411 Fall 2009 Final Exam Solution 1. (28 pts) Architectures a. Give an example of an area of computer architecture where bandwidth has improved faster than latency. How has this gap affected performance? Memory, storage, networks, etc. b. Describe how speculation can improve performance where dynamic scheduling cannot.

CMSC411 Fall 2009 Final Exam Solution

EEL 4713 – Computer Architecture Final Exam Friday, May 5th, 2006 NAME: Please read each question carefully, to avoid any confusion. This exam should have a total of 14 pages printed double-sided (pages 13 and 14 are scratch space). Before you begin, make sure your copy contains all pages. The exam is closed book, closed notes. Each question ...

EEL 4713 – Computer Architecture Final Exam

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Midterm 2 will be held in EHxxxx from 10:05am-12:05pm during the final exam slot on Monday, Dec. 16, 2019; Course Project Information. For the course project you will do a research-focused project. This may involve reimplementing an idea proposed in a paper we read in the class (or outside of class) or trying something new that you have come up ...

ECE/CS 752 Fall 2019

View full document Team Project 02 This is the Coursera Computer Architecture Course Final Exam Solution. To prepare for this assignment, the team must divide the viewing and analyzing of the Coursera 's Princeton University Computer Architecture classes (weeks 3 to 11).

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reliability measures and benchmarks, queuing theory, real faults, and failures. Practice Thread Level Parallelism MCQ PDF with answers to solve MCQ test questions: Thread level parallelism, shared memory architectures, GPU architecture issues, distributed shared memory and coherence, models of memory consistency, multicore processors and performance, symmetric shared memory multiprocessors, and synchronization basics.

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The Architecture of Computer Hardware, Systems Software and Networking is designed help students majoring in information technology (IT) and information systems (IS) understand the structure and operation of computers and computer-based devices. Requiring only basic computer skills, this accessible textbook introduces the basic principles of system architecture and explores current technological practices and trends using clear, easy-to-understand language. Throughout the text, numerous relatable examples, subject-specific illustrations, and in-depth case studies reinforce key learning points and show students how important concepts are applied in the real world. This fully-updated sixth edition features a wealth of new and revised content that reflects today ' s technological landscape. Organized into five parts, the book first explains the role of the computer in information systems and provides an overview of its components. Subsequent sections discuss the representation of data in the

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computer, hardware architecture and operational concepts, the basics of computer networking, system software and operating systems, and various interconnected systems and components. Students are introduced to the material using ideas already familiar to them, allowing them to gradually build upon what they have learned without being overwhelmed and develop a deeper knowledge of computer architecture.

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With growing interest in computer security and the protection of the code and data which execute on commodity computers, the amount of hardware security features in today's processors has increased significantly over the recent years. No longer of just academic interest, security features inside processors have been embraced by industry as well, with a number of commercial secure processor architectures available today. This book aims to give readers insights into the principles behind the design of academic and commercial secure processor architectures. Secure processor architecture research is concerned with exploring and designing hardware features inside computer processors, features which can help protect confidentiality and integrity of the code and data executing on the processor. Unlike traditional processor architecture research that focuses on performance, efficiency, and energy as the first-order design objectives, secure processor architecture design has security as the first-order design objective (while still keeping the others as important design aspects that need to be considered). This book aims to present the different challenges of secure processor architecture design to graduate students interested in research on architecture and hardware security and computer architects working in industry interested in adding security features to their designs. It aims to educate readers about how the different challenges have been solved in the past and what are the best practices, i.e., the principles, for design of new

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secure processor architectures. Based on the careful review of past work by many computer architects and security researchers, readers also will come to know the five basic principles needed for secure processor architecture design. The book also presents existing research challenges and potential new research directions. Finally, this book presents numerous design suggestions, as well as discusses pitfalls and fallacies that designers should avoid.

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