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circuit model and problem-driven parallel machines, variants of mesh architectures, and composite and hierarchical systems, among other ...

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Paperback. Computer Science. English. By (author) Behrooz Parhami. Share. Also available in. Hardback US\$191.94. THE CONTEXT OF PARALLEL PROCESSING The field of digital computer architecture has grown explosively in the past two decades. Through a steady stream of experimental research, tool-building efforts, and theoretical studies, the design of an instruction-set architecture, once considered an art, has been transformed into one of the most quantitative branches of computer technology.

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parallel processing. Some of the earliest parallel systems were designed by re-searchers in the field of fault-tolerant computing in order to allow independent multichannel computations and/or dynamic replacement of failed subsystems. These links are pointed out throughout the book. 5. Wide coverage of important topics.

Introduction to Parallel Processing - Lagout

The current text, Introduction to Parallel Processing: Algorithms and Architectures, is an outgrowth of lecture notes that the author has used for the graduate course "ECE 254B: Advanced Computer Architecture: Parallel Processing" at the University of California, Santa Barbara, and, in rudimentary forms, at several other institutions prior to 1988. The text has benefited greatly from keen observations, curiosity, and encouragement of my many students in these courses.

Behrooz Parhami's Textbook on Parallel Processing - UCSB

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THE CONTEXT OF PARALLEL PROCESSING The field of digital computer architecture has grown explosively in the past two decades. Through a steady stream of experimental research, tool-building efforts, and theoretical studies, the design of an instruction-set architecture, once considered an art, has been transformed into one of the most quantitative branches of computer technology. At the same time, better understanding of various forms of concurrency, from standard pipelining to massive parallelism, and invention of architectural structures to support a reasonably efficient and user-friendly programming model for such systems, has allowed hardware performance to continue its exponential growth. This trend is expected to continue in the near future. This explosive growth, linked with the expectation that performance will continue its exponential rise with each new generation of hardware and that (in stark contrast to software) computer hardware will function correctly as soon as it comes off the assembly line, has its down side. It has led to unprecedented hardware complexity and almost intolerable development costs. The challenge facing current and future computer designers is to institute simplicity where we now have complexity; to use fundamental theories being developed in this area to gain performance and ease-of-use benefits from simpler circuits; to understand the interplay between technological capabilities and limitations, on the one hand, and design decisions based on user and application requirements on the other.

This textbook is designed for the first course in Computer Architecture, usually offered at the junior/senior (3rd, 4th year) level in electrical engineering, computer science or computer engineering departments. This course is required of all electrical engineering and computer

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science/computer engineering majors specializing in the design of computer systems. This text provides a comprehensive introduction to computer architecture, covering topic from design of simple microprocessors to techniques used in the most advanced supercomputers.

Ideal for graduate and senior undergraduate courses in computer arithmetic and advanced digital design, *Computer Arithmetic: Algorithms and Hardware Designs, Second Edition*, provides a balanced, comprehensive treatment of computer arithmetic. It covers topics in arithmetic unit design and circuit implementation that complement the architectural and algorithmic speedup techniques used in high-performance computer architecture and parallel processing. Using a unified and consistent framework, the text begins with number representation and proceeds through basic arithmetic operations, floating-point arithmetic, and function evaluation methods. Later chapters cover broad design and implementation topics—including techniques for high-throughput, low-power, fault-tolerant, and reconfigurable arithmetic. An appendix provides a historical view of the field and speculates on its future. An indispensable resource for instruction, professional development, and research, *Computer Arithmetic: Algorithms and Hardware Designs, Second Edition*, combines broad coverage of the underlying theories of computer arithmetic with numerous examples of practical designs, worked-out examples, and a large collection of meaningful problems. This second edition includes a new chapter on reconfigurable arithmetic, in order to address the fact that arithmetic functions are increasingly being implemented on field-programmable gate arrays (FPGAs) and FPGA-like configurable devices. Updated and thoroughly revised, the book offers new and expanded coverage of saturating adders and multipliers, truncated multipliers, fused multiply-add units, overlapped quotient digit selection, bipartite and multipartite tables, reversible logic, dot notation, modular arithmetic, Montgomery modular reduction, division by constants, IEEE floating-point standard formats, and interval arithmetic. Features: * Divided into 28 lecture-size chapters * Emphasizes both the underlying theories of computer arithmetic and actual hardware designs * Carefully links computer arithmetic to other subfields of computer engineering * Includes 717 end-of-chapter problems ranging in complexity from simple exercises to mini-projects * Incorporates many examples of practical designs * Uses consistent standardized notation throughout * Instructor's manual includes solutions to text problems * An author-maintained website http://www.ece.ucsb.edu/~parhami/text_comp_arit.htm contains instructor resources, including complete lecture slides

Sustainable Wireless Network-on-Chip Architectures focuses on developing novel Dynamic Thermal Management (DTM) and Dynamic Voltage and Frequency Scaling (DVFS) algorithms that exploit the advantages inherent in WiNoC architectures. The methodologies proposed—combined with extensive experimental validation—collectively represent efforts to create a sustainable NoC architecture for future many-core chips. Current research trends show a necessary paradigm shift towards green and sustainable computing. As implementing massively parallel energy-efficient CPUs and reducing resource consumption become standard, and their speed and power continuously increase, energy issues become a significant concern. The need for promoting research in sustainable computing is imperative. As hundreds of cores are integrated in a single chip, designing effective packages for dissipating maximum heat is infeasible. Moreover, technology scaling is pushing the limits of affordable cooling, thereby requiring suitable design techniques to reduce peak temperatures. Addressing thermal concerns at different design stages is critical to the success of future generation systems. DTM and DVFS appear as solutions to avoid high spatial and temporal temperature variations among NoC components, and thereby mitigate local network hotspots. Defines new complex, sustainable network-on-chip architectures to reduce network latency and energy Develops topology-agnostic dynamic thermal management and dynamic voltage

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and frequency scaling techniques Describes joint strategies for network- and core-level sustainability Discusses novel algorithms that exploit the advantages inherent in Wireless Network-on-Chip architectures

You too can learn to design and develop classic arcade video games like Pong, Pac-Man, Space Invaders, and Scramble. Collision detection, extra lives, power-ups, and countless other essential design elements were invented by the mostly anonymous designers at the early pioneering companies that produced these great games. In this book you'll go step by step, using modern, free software tools such as Unity3D to create five games in the classic style, inspired by these classics: Pong, Breakout, Space Invaders, Scramble, and Pac-Man. All the source code, art and sound sources for the projects are freely available on the companion DVD or at the book's Web site. You'll discover the fun of making your own games, putting in your own color graphics, adjusting the scoring, coding the AI, and creating the sound effects. You'll gain a deep understanding of the roots of modern video game design: the classics of the seventies and eighties. Features: * Uses seven Unity3D projects to allow for quick experimentation with classic game concepts * 4-color throughout with companion DVD that includes source code, art, and full projects * Includes historical anecdotes direct from one of the fabled Atari coin-op programmers * Detailed step-by-step instructions, dozens of exercises, and eight rules of classic game design * Contains unique insights on applying classic game design concepts to modern games

Build real-world applications with Python 2.7, CUDA 9, and CUDA 10. We suggest the use of Python 2.7 over Python 3.x, since Python 2.7 has stable support across all the libraries we use in this book. Key Features Expand your background in GPU programming—PyCUDA, scikit-cuda, and Nsight Effectively use CUDA libraries such as cuBLAS, cuFFT, and cuSolver Apply GPU programming to modern data science applications Book Description Hands-On GPU Programming with Python and CUDA hits the ground running: you'll start by learning how to apply Amdahl's Law, use a code profiler to identify bottlenecks in your Python code, and set up an appropriate GPU programming environment. You'll then see how to "query" the GPU's features and copy arrays of data to and from the GPU's own memory. As you make your way through the book, you'll launch code directly onto the GPU and write full blown GPU kernels and device functions in CUDA C. You'll get to grips with profiling GPU code effectively and fully test and debug your code using Nsight IDE. Next, you'll explore some of the more well-known NVIDIA libraries, such as cuFFT and cuBLAS. With a solid background in place, you will now apply your new-found knowledge to develop your very own GPU-based deep neural network from scratch. You'll then explore advanced topics, such as warp shuffling, dynamic parallelism, and PTX assembly. In the final chapter, you'll see some topics and applications related to GPU programming that you may wish to pursue, including AI, graphics, and blockchain. By the end of this book, you will be able to apply GPU programming to problems related to data science and high-performance computing. What you will learn Launch GPU code directly from Python Write effective and efficient GPU kernels and device functions Use libraries such as cuFFT, cuBLAS, and cuSolver Debug and profile your code with Nsight and Visual Profiler Apply GPU programming to datascience problems Build a GPU-based deep neuralnetwork from scratch Explore advanced GPU hardware features, such as warp shuffling Who this book is for Hands-On GPU Programming with Python and CUDA is for developers and data scientists who want to learn the basics of effective GPU programming to improve performance using Python code. You should have an understanding of first-year college or university-level engineering mathematics and physics, and have some experience with Python as well as in any C-based programming language such as C, C++, Go, or Java.

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This book focuses on the future directions of the static scheduling and dynamic load balancing methods in parallel and distributed systems. It provides an overview and a detailed discussion of a wide range of topics from theoretical background to practical, state-of-the-art scheduling and load balancing techniques.

This book describes warehouse-scale computers (WSCs), the computing platforms that power cloud computing and all the great web services we use every day. It discusses how these new systems treat the datacenter itself as one massive computer designed at warehouse scale, with hardware and software working in concert to deliver good levels of internet service performance. The book details the architecture of WSCs and covers the main factors influencing their design, operation, and cost structure, and the characteristics of their software base. Each chapter contains multiple real-world examples, including detailed case studies and previously unpublished details of the infrastructure used to power Google's online services. Targeted at the architects and programmers of today's WSCs, this book provides a great foundation for those looking to innovate in this fascinating and important area, but the material will also be broadly interesting to those who just want to understand the infrastructure powering the internet. The third edition reflects four years of advancements since the previous edition and nearly doubles the number of pictures and figures. New topics range from additional workloads like video streaming, machine learning, and public cloud to specialized silicon accelerators, storage and network building blocks, and a revised discussion of data center power and cooling, and uptime. Further discussions of emerging trends and opportunities ensure that this revised edition will remain an essential resource for educators and professionals working on the next generation of WSCs.

Designed as an introductory text for the students of computer science, computer applications, electronics engineering and information technology for their first course on the organization and architecture of computers, this accessible, student friendly text gives a clear and in-depth analysis of the basic principles underlying the subject. This self-contained text devotes one full chapter to the basics of digital logic. While the initial chapters describe in detail about computer organization, including CPU design, ALU design, memory design and I/O organization, the text also deals with Assembly Language Programming for Pentium using NASM assembler. What distinguishes the text is the special attention it pays to Cache and Virtual Memory organization, as well as to RISC architecture and the intricacies of pipelining. All these discussions are climaxed by an illuminating discussion on parallel computers which shows how processors are interconnected to create a variety of parallel computers. KEY FEATURES ? Self-contained presentation starting with data representation and ending with advanced parallel computer architecture. ? Systematic and logical organization of topics. ? Large number of worked-out examples and exercises. ? Contains basics of assembly language programming. ? Each chapter has learning objectives and a detailed summary to help students to quickly revise the material.

The Encyclopedia of Big Data Technologies provides researchers, educators, students and industry professionals with a comprehensive authority over the most relevant Big Data Technology concepts. With over 300 articles written by worldwide subject matter experts from both industry and academia, the encyclopedia covers topics such as big data storage systems, NoSQL database, cloud computing, distributed systems, data processing, data management, machine learning and social technologies, data science. Each peer-reviewed, highly structured entry provides the reader with basic terminology, subject overviews, key research results, application examples, future directions, cross references and a bibliography. The entries are expository and tutorial, making this reference a practical resource for students, academics, or

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