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The material covered includes the algorithms used in circuit simulation and the numerical techniques needed for linear and non-linear DC analysis, transient analysis and AC analysis. The book goes on to explain the numeric methods to include sensitivity and tolerance analysis and optimisation of component values for circuit design.

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Optimization | V. Litovski ...

Simulation tools are needed to extract the electrical characteristics of your circuit blocks for VLSI. CMOS VLSI design is the first step in creating a silicon wafer with dozens of ICs. CMOS (complementary metal-oxide-semiconductor) VLSI (very-large-scale integration) design has enabled massive scaling in a variety of semiconductor devices.

CMOS VLSI Design and Circuit Simulation Tasks

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The material covered includes the algorithms used in circuit simulation and the numerical techniques needed for linear and non-linear DC analysis, transient analysis and AC analysis. The book goes on to explain the numeric methods to include sensitivity and tolerance analysis and optimisation of component values for circuit design.

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Emphasis is given to circuit analysis, timing verification and optimization since simulation is covered by C. Terman in this book. Also, the optimization of large circuits is receiving new attention due to the need for timing performance improvement in silicon compilation. This is a preview of subscription content, log in to check access.

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VLSI Circuit Simulation and Optimization by Litovski, V ...

Abstract Designers of digital VLSI circuits have virtually no computer tools available for the optimization of circuit performance. Instead, a designer relies extensively on circuit-analysis tools, such as circuit simulation (SPICE) and/or critical-delay-path analysis.

Performance optimization of digital VLSI circuits (Thesis ...

circuit simulation. The inter-algorithm parallelism approach in HMAPS is completely di erent from the existing intra-algorithm parallel circuit simulation techniques and achieves superlinear speedup in practice. The second part of the dissertation talks about parallel circuit optimization. A modified asynchronous parallel pattern search

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Parallel VLSI Circuit Analysis and Optimization

The penalty was that power dissipation became a critical parameter in digital VLSI design. This paper puts an insight into the various sources of power dissipation in digital CMOS and the power optimization techniques at circuit and device level.

Circuit simulation has become an essential tool in circuit design and without it's aid, analogue and mixed-signal IC design would be impossible. However the applicability and limitations of circuit simulators have not been generally well understood and this book now provides a clear and easy to follow explanation of their function. The material covered includes the algorithms used in circuit simulation and the numerical techniques needed for linear and non-linear DC analysis, transient analysis and AC analysis. The book goes on to explain the numeric methods to include sensitivity and tolerance analysis and optimisation of component values for circuit design. The final part deals with logic simulation and mixed-signal simulation algorithms. There are comprehensive and detailed descriptions of the numerical methods and the material is presented in a way that provides for the needs of both experienced engineers who wish to extend their knowledge of current tools and techniques, and of advanced students and researchers who wish to develop new simulators.

The prevalence of multi-core processors in recent years has introduced new opportunities and challenges to Electronic Design Automation (EDA) research and development. In this dissertation, a few parallel Very Large Scale Integration (VLSI) circuit analysis and optimization methods which utilize the multi-core computing platform to tackle some of the most difficult contemporary Computer-Aided Design (CAD) problems are presented. The first CAD application that is addressed in this dissertation is analyzing and optimizing mesh-based clock distribution network. Mesh-based clock distribution network (also known as clock mesh) is used in high-performance microprocessor designs as a reliable way of distributing clock signals to the entire chip. The second CAD application addressed in this dissertation is the Simulation Program with Integrated Circuit Emphasis (SPICE) like circuit simulation. SPICE simulation is often regarded as the bottleneck of the design flow. Recently, parallel circuit simulation has attracted a lot of attention. The first part of the dissertation discusses circuit analysis techniques. First, a combination of clock network specific model order reduction algorithm and a port sliding scheme is presented to tackle the challenges in analyzing large clock meshes with a large number of clock drivers. Our techniques run much faster than the standard SPICE simulation and existing model order reduction techniques. They also provide a basis for the clock mesh optimization. Then, a hierarchical multialgorithm parallel circuit simulation (HMAPS) framework is presented as an novel technique of parallel circuit simulation. The inter-algorithm parallelism approach in HMAPS is completely different from the existing intra-algorithm parallel circuit simulation techniques and achieves superlinear speedup in practice. The second part of the dissertation talks about parallel circuit optimization. A modified asynchronous parallel pattern search (APPS) based method which utilizes the efficient clock mesh simulation techniques for the clock driver size optimization problem is presented. Our modified APPS method runs much faster than a continuous optimization method and effectively reduces the clock skew for all test circuits. The third part of the dissertation describes parallel performance modeling and optimization of the HMAPS framework. The performance models and runtime optimization scheme improve the speed of HMAPS further more. The dynamically adapted HMAPS becomes a complete solution for parallel circuit simulation.

This book describes new, fuzzy logic-based mathematical apparatus, which enable readers to work with continuous variables, while implementing whole circuit simulations with speed, similar to gate-level simulators and accuracy, similar to circuit-level simulators. The author demonstrates newly developed principles of digital integrated circuit simulation and optimization that take into consideration various external and internal destabilizing factors, influencing the operation of digital ICs. The discussion includes factors including radiation, ambient temperature, electromagnetic fields, and climatic conditions, as well as non-ideality of interconnects and power rails.

Metal Oxide Semiconductor (MOS) transistors are the basic building block ofMOS integrated circuits (I C). Very Large Scale Integrated (VLSI) circuits using MOS technology have emerged as the dominant technology in the semiconductor industry. Over the past decade, the complexity of MOS IC's has increased at an astonishing rate. This is realized mainly through the reduction of MOS transistor dimensions in addition to the improvements in processing.

Today VLSI circuits with over 3 million transistors on a chip, with effective or electrical channel lengths of 0. 5 microns, are in volume production. Designing such complex chips is virtually impossible without simulation tools which help to predict circuit behavior before actual circuits are fabricated. However, the utility of simulators as a tool for the design and analysis of circuits depends on the adequacy of the device models used in the simulator. This problem is further aggravated by the technology trend towards smaller and smaller device dimensions which increases the complexity of the models. There is extensive literature available on modeling these short channel devices. However, there is a lot of confusion too. Often it is not clear what model to use and which model parameter values are important and how to determine them. After working over 15 years in the field of semiconductor device modeling, I have felt the need for a book which can fill the gap between the theory and the practice of MOS transistor modeling. This book is an attempt in that direction.

As MOS devices are scaled to

meet increasingly demanding circuit specifications, process variations have a greater effect on the reliability of circuit performance. For this reason, statistical techniques are required to design integrated circuits with maximum yield. Statistical Modeling for Computer-Aided Design of MOS VLSI Circuits describes a statistical circuit simulation and optimization environment for VLSI circuit designers. The first step toward accomplishing statistical circuit design and optimization is the development of an accurate CAD tool capable of performing statistical simulation. This tool must be based on a statistical model which comprehends the effect of device and circuit characteristics, such as device size, bias, and circuit layout, which are under the control of the circuit designer on the variability of circuit performance. The distinctive feature of the CAD tool described in this book is its ability to accurately model and simulate the effect in both intra- and inter-die process variability on analog/digital circuits, accounting for the effects of the aforementioned device and circuit characteristics. Statistical Modeling for Computer-Aided Design of MOS VLSI Circuits serves as an excellent reference for those working in the field, and may be used as the text for an advanced course on the subject.

This book covers algorithmic aspects of computer aided circuit design for VLSI of large circuits. The large scale aspect of VLSI requires a reorientation towards new and more efficient techniques. Many algorithms have survived the test of time, while others are suffering from the usual problem of polynominal or exponential running time complexity and storage requirements. The approaches presented in this book are techniques which were developed in response to the VLSI problems. The most recent ``exact'' circuit analysis and simulation techniques are presented, such as waveform relaxation and timing simulation. The book concentrates on the analysis and simulation of large circuits which exceed the capabilities of general purpose analyzers in both compute time and storage. Also discussed are circuit models for switch level simulation, techniques and circuit models for interconnections, capacitance and inductances and optimization techniques. The language and notation have been kept uniform throughout the book to help the reader to maintain the continuity between the topics discussed in the different chapters. All algorithms are written in a Pascal style. The terminology used should reflect the emerging language used in most of the VLSI circuit design community. The book includes proven approaches as well as techniques which are presently in a research state.

This book constitutes the refereed proceedings of the 17th International Symposium on VLSI Design and Test, VDAT 2013, held in Jaipur, India, in July 2013. The 44 papers presented were carefully reviewed and selected from 162 submissions. The papers discuss the frontiers of design and test of VLSI components, circuits and systems. They are organized in topical sections on VLSI design, testing and verification, embedded systems, emerging technology.

This book constitutes the thoroughly refereed postconference proceedings of 19th International Workshop on Power and Timing Modeling, Optimization and Simulation, PATMOS 2009, featuring Integrated Circuit and System Design, held in Delft, The Netherlands during September 9-11, 2009. The 26 revised full papers and 10 revised poster papers presented were carefully reviewed and selected from numerous submissions. The papers are organized in topical sections on variability & statistical timing, circuit level techniques, power management, low power circuits & technology, system level techniques, power & timing optimization techniques, self-timed circuits, low power circuit analysis & optimization, and low power design studies.

A reprint of the classic text, this book popularized compact modeling of electronic and semiconductor devices and components for college and graduate-school classrooms, and manufacturing engineering, over a decade ago. The first comprehensive book on MOS transistor compact modeling, it was the most cited among similar books in the area and remains the most frequently cited today. The coverage is device-physics based and continues to be relevant to the latest advances in MOS transistor modeling. This is also the only book that discusses in detail how to measure device model parameters required for circuit simulations. The book deals with the MOS Field Effect Transistor (MOSFET) models that are derived from basic semiconductor theory. Various models are developed, ranging from simple to more sophisticated models that take into account new physical effects observed in submicron transistors used in today's (1993) MOS VLSI technology. The assumptions used to arrive at the models are emphasized so that the accuracy of the models in describing the device characteristics are clearly understood. Due to the importance of designing reliable circuits, device reliability models are also covered. Understanding these models is essential when designing circuits for state-of-the-art MOS ICs.